9. (New) The power semiconductor device according to Claim 8, wherein a thickness of said lower pattern is 0.2 mm of less.

10. (New) The power semiconductor device according to Claim 9, wherein a thickness of said soldering layer is 100 to 300 μm.

11. (New) The power semiconductor device according to Claim 8, wherein a thickness of said lower pattern is 0.1 mm or less.

12. (New) The power semiconductor device according to Claim 11, wherein a thickness of said soldering layer is 50 to 400 μm.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-3, 5-6 and 8-12 are presented for examination. Claim 1 has been amended to better clarify the present invention without the introduction of any new matter. Claims 4 and 7 have been canceled without prejudice or disclaimer and Claims 8-12 have been added. New Claim 8 incorporates the limitations of Claims 1 and 4 with the uniformity discussed at page 9, line 20 - page 10, line 4 of the specification, for example. New Claims 9-12 correspond to Claims 2, 3, 5 and 6 but dependent on Claim 8.

The outstanding Office Action presents a rejection of Claims 1-7 under 35 U.S.C. § 103(a) over Terasawa (U.S. Patent No. 5,942,747) in view of Braden et al (U.S. Patent No. 5,504,372, Braden).

Before considering this outstanding obviousness rejection, it is believed that a brief review of the present invention would be helpful. In this regard, the present invention is concerned with a power semiconductor device that includes a ceramic substrate having a thickness of 0.5 to 1 mm. An aluminum alloy is provided on an upper main surface of this

ceramic substrate that has a thickness of 0.4 to 0.6 mm to which a power semiconductor element is connected. The ceramic substrate has a lower main surface provided with a lower pattern made of an aluminum alloy that is spaced opposite to a metal base plate made of a copper alloy that has a thickness of from 3.5 to 5.5 mm. A soldering layer is formed between the entire surface of the lower pattern and the metal base plate in order to form a joint therebetween. As noted, for example, at page 2, line 18 through page 3, line 2, and page 7, line 14 through page 8, line 9, the structure of the present invention provides many improved results and mitigates problems in previously known devices. Furthermore, the particular dimensions employed ensure reduced cracking and that an inexpensive copper alloy can be used instead of more costly materials for the metal base plate.

Turning to the outstanding rejection of Claims 1-7, base independent Claim 1 clearly requires the circuit pattern provided on the upper surface of the ceramic substrate and the lower pattern on the lower main surface of the ceramic substrate opposite to the upper main surface to both be made of an aluminum alloy. In addition, Claim 1 requires that the soldering layer must be provided between an entire surface of the lower pattern and metal base plate for forming a joint therebetween. The outstanding Office Action improperly address these two differences by first improperly asserting that Braden teaches aluminum and copper alloys in the formation of metallic films. It then improperly asserts that Terasawa teaches placing a soldering layer between an entire surface of a lower pattern and a metal base plate.

Turning first to the second incorrect assertion, it is noted that col. 5, lines 63+ of Terasawa are relied upon in the outstanding Office Action. However, the only thing taught at col. 5, lines 63+ is that "lower copper plate 23 is soldered to the metal base plate 10." There is no teaching here to use a sufficient amount of solder to form a solder layer between an

entire surface of the lower pattern and the metal base plate for forming a joint therebetween. The Office Action appears to be improperly relying upon an assumption that is made not a teaching that appears in the reference. Merely because the lower copper plate 23 is soldered to the metal base plate 10, this could be accomplished by one or more solder joints that do not cover all of surface of the lower pattern and, thus, cannot be said to be a teaching that an entire surface of this lower copper plate 23 is soldered to the metal base plate 10.

In addition to there being no fair teaching in Terasawa of this required provision of the soldering layer between the entire surface of the lower pattern in the metal base plate, there is further no teaching in Braden of an aluminum alloy being used in the formation of "metallic films" as alleged at the middle of pate 3 of the outstanding Office Action. In this regard, the formation of copper films is not relevant to Claim 1 subject matter. Moreover, the base component 12 and cover component 14 discussed at col. 3, lines 54-56 of Braden are clearly illustrated in Figure 1 as being components of the case and in no way reasonably readable as any kind of "metallic film." While col. 4, lines 5-12 of Braden discuss different wires made of different metal alloys including aluminum and copper, these bonded wires are clearly not "metallic films," and certainly not aluminum films. The "thin strips of copper foil that can be used as indicated at col. 4, lines 13-15 of Braden, are clearly not aluminum alloys. Turning to col. 6, lines 18-34 of Braden, aluminum base alloy is suggested for metallic base component 12, but 12 is again not a metallic film. Similarly, the metallic base component 12 of copper or copper base alloy of col. 6, line 35 of Braden is not a "metallic film." Accordingly, even if aluminum is mixed with this copper as suggested at col. 6, lines 44-47, the resulting base component 12 is not reasonably or fairly characterized as a "metallic film."

Moreover, neither of the applied references have even the remotest suggestion of achieving the improved results of the present invention stemming from the particular

thicknesses of the aluminum alloy used. In this regard, the paragraph bridging pages 3 and 4 of the outstanding Office Action has attempted to rely upon the Aller decision cited there as authorizing the rejection of any recited claimed range as being a matter of routine experimentation. However, as explained in In re Antonie, 195 USPQ 6, 8 (CCPA 1977), before it can be said to be obvious to optimize a result-effective variable, the PTO must establish that the artisan would have known the particular parameter was a result-effective variable, i.e., a variable which achieves a recognized result. Nothing in any of the references applied demonstrate any realization in the prior art that the particular thicknesses of the aluminum alloy layers relative to the other layers have any effect that is advantageous.

Accordingly, the rejection of Claim 1 over the combined teachings of Terasawa and Braden is respectfully traversed.

Turning to Claims 2, 3, 5, and 6, it is noted that each of these claims is ultimately dependent on base Claim 1 and, accordingly, defines over the applied references for at least the reasons that Claim 1 does. In addition, each of these dependent claims set forth further features that are clearly not taught or suggested by either Terasawa or Braden whether these references be considered alone or together in any proper combination. Accordingly, each of Claims 2, 3, 5, and 6 is further considered patentable because of the additional features that each of these dependent claims adds to the subject matter of the common base Claim 1.

With regard to new Claim 8, it is noted that this claim includes all the limitations of Claim 1 with the added requirement for uniformity of spacing provided by a wire bump. New Claim 8 is believed to be clearly patentable for the reasons discussed above as to Claim 1 and also because Terasawa and/or Braden, considered alone or together in any proper combination, also fail to teach or suggest the additional Claim 8 subject matter.

New Claims 9-12 depend ultimately on Claim 8 and, accordingly, are patentable at least for the same reasons Claim 8 is.

As no further issues are believed to be outstanding relative to this application, it is believed that this application is clearly in condition for formal allowance and an early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please amend the specification as follows:

Please replace the paragraph beginning on page 1, line 25 to page 2, line 7, with the following text:

--When a Cu alloy is used as the material for the circuit pattern and the lower pattern, there is a high probability of cracks [may be caused] forming in the insulating substrate and the soldering layer [with a high probability] in an early stage due to a temperature cycle. As a countermeasure for this problem, Al/SiC and Cu/Mo [having expansion coefficients more approximate to that of ceramics used as the material for the insulating substrate than that of Cu] may be used as the materials for the metal base plate instead of Cu as these materials have coefficients of expansion closer to that of the ceramics being used. While reliability of the power semiconductor device is improved by using Al/SiC and Cu/Mo for the metal base plate, these materials have a disadvantage of being more costly than [a] Cu [alloy].--

Please replace the paragraph beginning on page 2, lines 8-12, with the following text:

--When an Al alloy is used as the material for the circuit pattern and the lower pattern, instead of Cu, [on the other hand,] the resistance to cracks of the insulating substrate [made of ceramics to cracks] can be improved. However, [it is not expected to avoid] cracks [to be] caused in the soldering layer in [an] the above-noted early stage due to a temperature cycle

are not eliminated by this alternative. [For this reason, Al/SiC and Cu/Mo are yet used as the materials for the metal base plate.]--

Please replace the paragraph beginning on page 2, lines 13-17, with the following text:

--[Especially] Moreover, when the lower pattern is made of an Al alloy having a thickness of 0.4 to 0.5 mm, electrical resistance is increased as compared with the electrical resistance of a lower patter made of a Cu alloy. [The] This increase in electrical resistance results in an increase in heat resistance of the power semiconductor device as a whole, to thereby reduce the heat dissipation capacity of a semiconductor element to be mounted on the insulating substrate.--

Please replace the paragraph beginning on page 2, line 18 to page 3, line 2, with the following text:

--Further, as [a] the thickness of the soldering layer [is] has been arbitrarily set, and there has been no concern as to the soldering layer [is] being defined to have a nonuniform thickness, [Therefore] the insulating substrate may be inclined at a junction between the lower pattern and the metal base plate, [inducing the] causing heat resistance to increase. Consequently, it is probable that a balance between target heat resistance and resistance of the soldering layer to cracks may be lost, resulting in the problems of increased dispersion of a quality, change of design and decreased tolerance of design. A further problem [may be caused] is that the above-noted cracks due to a temperature cycle are likely to occur in the soldering layer at its corner portions that are of a thinned thickness in [an] the above-noted early stage. This problem may result in increased heat resistance, to thereby destroy the power semiconductor element.--

Please replace the paragraph beginning on page 3, lines 5-14, with the following text:

--A first aspect of the present invention is directed to a power semiconductor device, comprising: a ceramic substrate having a thickness of 0.5 to 1 mm; a circuit pattern made of an aluminum alloy and provided on an upper main surface of the ceramic substrate and having a thickness of 0.4 to 0.6 mm on which a power semiconductor element is held; a lower pattern made of the aluminum alloy [having a thickness of 0.2 mm or less and] provided entirely on a lower main surface of the ceramic substrate opposite to the upper main surface; a metal base plate of a copper alloy having a thickness of 3.5 to 5.5 mm [to be opposite] opposes the lower pattern; and a soldering layer [having thickness of 100 to 300 μm and] provided between an entire surface of the lower pattern and the metal base plate for forming a joint therebetween.--

Please replace the paragraph beginning on page 3, lines 15-24, with the following text:

--A second aspect of the present invention is directed to a power semiconductor device, comprising: a ceramic substrate having a thickness of 0.5 to 1 mm; a circuit pattern made of an aluminum alloy and provided on an upper main surface of the ceramic substrate [to grow to] with a thickness of 0.4 to 0.6 mm for holding a power semiconductor element thereon; a lower pattern formed of a metalized layer having a thickness of 0.1 mm or less and provided entirely on a lower main surface of the ceramic substrate opposite to the upper main surface; a metal base plate made of a copper alloy having a thickness of 3.5 to 5.5 mm [to be] opposite to the lower pattern; and a soldering layer having [a] uniform thickness of 50 to 400 μm [and] is provided between an entire surface of the lower pattern and the metal base plate for forming a joint therebetween.--

Please replace the paragraph beginning on page 4, lines 3-5, with the following text:

--According to the first aspect of the present invention, it is possible to provide a power semiconductor device excellent [having excellence] in heat dissipation capacity and heat cycle.--

Please replace the paragraph beginning on page 4, lines 6-9, with the following text:

--According to the second aspect of the present invention, as the lower pattern is formed of the metalized layer, the soldering layer as well as the lower pattern can be reduced in thickness. As a result, it is possible to provide an inexpensive power semiconductor device [having excellence] excellent in heat dissipation capacity and productivity.--

Please replace the paragraph beginning on page 4, lines 10-16, with the following text:

--According to the third aspect of the present invention, it is possible to prevent the ceramic substrate from being inclined at a junction between the lower pattern and the metal base plate. Further, [a space] uniform spacing between the lower pattern and the metal base plate can be ensured. In addition, the thickness of the soldering layer is [likely to be uniformalized,] made uniform to enable the soldering layer to be [easily] reduced in thickness. As a result, [excellence in] excellent productivity and [considerably] high [effectiveness in] cost reduction can be obtained.--

Please replace the paragraph beginning on page 4, lines 17-20, with the following text:

--It is an object of the present invention to provide a power semiconductor device having a circuit pattern and a lower pattern made of an Al alloy for cost reduction and enabling reduction in heat resistance and improvement in resistance of a soldering layer as to cracking during a heat cycle.--

Please replace the paragraph beginning on page 5, line 5, with the following text:

--Fig. 3 is a graph showing [structures of] comparative data as to the present invention.--

Please replace the paragraph beginning on page 5, lines 8-9, with the following text:

--Fig. 1 is a cross-sectional view illustrating a power semiconductor device that is commonly applicable to the preferred embodiment described later.--

Please replace the paragraph beginning on page 6, lines 11-14, with the following text:

--Fig. 3 is a graph showing [structures of] comparative data as to the present invention. A group of t_2 lines enclosed by L1 refers to dependence of distortion ϵ (absolute number) [to occur] occurring in the soldering layer 8C due to a heat cycle [and a] on the thickness t_3 of soldering layer 8C. The group of lines t_2 enclosed by L2 refers to dependence of heat resistance R_{th} ($°C/W$), [both] on the thickness t_3 of the soldering layer 8C.--

Please replace the paragraph beginning on page 6, lines 15-17, with the following text:

--[A] The heat cycle requires temperature ranging from -40 to 125°C. The target number of times of heat cycles is 1000 to 1500 cycles in power modules for electric railways and automobiles requiring high reliability.--

Please replace the paragraph beginning on page 6, line 18 to page 7, line 4, with the following text:

--In the group of t_2 lines enclosed by L1[,] (L11, line L12, line L13 and line L14) show the selection of the thickness t_2 of the lower pattern 5 of 0.1 mm, 0.2 mm, 0.3 mm and 0.4 mm, respectively. In the group of t_2 lines enclosed by L2[,] (line L21, line L22, line L23 and line L24) show the selection of the thickness t_2 of the lower pattern 5 of 0.1 mm, 0.2 mm, 0.3 mm and 0.4 mm, respectively. When Al foil is joined as the lower pattern 5 on the

insulating substrate 3 made of ceramics, a lower limit of the thickness t_2 may be around 0.1 mm. There occurs little fluctuation in lines L11, L12, L13, L14, L21, L22, L23 and L24 by the thickness of the metal base plate 1, the insulating substrate 3 and the circuit pattern 4 falling within the ranges thereof as mentioned above. For comparison, line L19 and line L29 defined by the circuit pattern 4 and the lower pattern 5 made of a Cu alloy are added to the group of t_2 lines enclosed by L1 and L2, respectively. More particularly, the circuit pattern 4 grows to a thickness of 0.3 mm and the lower pattern 5 grows to a thickness of 0.15 mm.--

Please replace the paragraph beginning on page 7, lines 5-13, with the following text:

--As the thickness t_3 of the soldering layer 8C increases and as the thickness t_2 of the lower pattern 5 decreases, the distortion ε [to occur] occurring in the soldering layer 8C is reduced. In order to obtain the distortion ε that is smaller than the distortion occurring [in the case using] when a Cu alloy is used as the circuit pattern 4 and the lower pattern 5 (line L19), the thickness t_2 [is desired to] should be 0.1 mm (line L11) when an Al alloy is used as the lower pattern 5. However, in order to [obtain] ensure the distortion ε [to occur] in the soldering layer 8C [having] has a value smaller than [a] the illustrated permissible value ε_0, the thickness t_3 of the soldering layer 8C is required to be 100 μm or more when the thickness t_2 of the lower patter 5 is 0.1 mm.--

Please replace the paragraph beginning on page 7, line 25 to page 8, line 8, with the following text:

--In view of the foregoing, when both of the circuit pattern 4 and the lower pattern 5 are made of an Al alloy and when the thickness of the metal base plate 1, the insulating substrate 3 and the circuit pattern 4 fall within the ranges as mentioned above, for example, the thickness t_3 of the soldering layer 8C is set to fall within the range of 100 to 300 μm with the lower pattern 5 having the thickness t_2 of 0.2 mm or less to thereby control the distortion

ε and the heat resistance R_{th} favorably. Therefore, a power semiconductor device [having excellence] excellent in heat dissipation capacity and heat cycle can be provided. Further, the metal base plate 1 can be made of an inexpensive Cu alloy instead of costly Al/SiC and Cu/Mo.--

Please replace the paragraph beginning on page 8, line 17 to page 9, line 4, with the following text:

--Both of line L10 belonging to the group of t_2 lines L1 and line L20 belonging to the group of t_2 lines L2 are defined by the lower pattern 5 formed of a metalized layer. There occurs little fluctuation in lines L10 and L20 [by] due to the thickness of the metal base [pate] plate 1, the insulating substrate 3 and the circuit pattern 4 under the condition that these thicknesses fall within the ranges thereof [as] mentioned above. Such a metalized layer is formed using known metalizing techniques such as spraying or vapor deposition to [grow to] provide a thickness of 0.005 to 0.1 mm, or preferably, 0.020 mm or less. As materials for the metalized layer, Mo-Mn (molybdenum-manganese) and W (tungsten) are applicable. Alternatively, a brazing material such as an Al-based material to be provided between the circuit pattern 4 and the insulating substrate 3 is applicable. In any case, in order to improve adhesion and wettability to the soldering layer 8C, it is desirable to plate the surface of the metalized layer, namely, the side to be joined onto the metal base plate 1, with Ni (nickel) plating.--

Please replace the paragraph beginning on page 9, lines 15-18, with the following text:

--In view of the foregoing, the thickness of the soldering layer 8C can be small [as well] according to this preferred embodiment. As a result, it is possible to provide an

inexpensive power semiconductor device [having excellence] excellent in heat dissipation capacity and productivity.--

Please replace the paragraph beginning on page 9, lines 20-23, with the following text:

--As shown in Figs. 1 and 2, wire bumps 9 made of Al or the like are sandwiched between the lower pattern 5 and the metal base plate 1 to be in contact with the soldering layer 8C. A space between the metal base plate and the substrate 2 of semiconductor elements can be [uniformalized by] made uniform using these wire bumps 9.--

Please replace the paragraph beginning on page 9, line 24 to page 10, line 4, with the following text:

--The insulating substrate 3 can be thereby prevented from being inclined at a junction between the lower pattern 5 and the metal base plate 1. Further, [a space] uniform spacing between the lower pattern 5 and the metal base plate 1 can be ensured. In addition, the thickness of the soldering layer 8C is [likely to be uniformalized,] made uniform to enable the soldering layer 8C to be easily reduced in thickness. As a result, [excellence in] excellent productivity and effective [considerably high effectiveness in] cost reduction can be obtained.--

Please replace the paragraph beginning on page 10, lines 5-8, with the following text:

--In consideration of heat dissipation capacity and reliability, diameters of the wire bumps 9 are desirably about 50 to 400 μm. Consequently, it is [a matter of course] clear that the wire bumps 9 are further applicable to the aforementioned first and second preferred embodiments.--

IN THE CLAIMS

Please amend Claim 1 as follows:

--1. (Amended) A power semiconductor device comprising:

a ceramic substrate having a thickness of 0.5 to 1 mm;

a power semiconductor element;

a circuit pattern made of an aluminum alloy and provided on an upper main surface of said ceramic substrate and having a thickness 0.4 to 0.6 mm on which said power semiconductor element is held;

a lower pattern made of said aluminum alloy and provided entirely on a lower main surface of said ceramic substrate opposite to said upper main surface;

a metal base plate made of a copper alloy having a thickness of 3.5 to 5.5 mm [to be] positioned opposite to said lower pattern; and

a soldering layer provided between an entire surface of said lower pattern and said metal base plate for forming a joint therebetween.

4. (Canceled)

7. (Canceled)

8. (New)

9. (New)

10. (New)

11. (New)

12. (New)